

Liberate MX

Improve your view...

Liberate MX extends Altos' ultra-fast standard cell and I/O library characterization capabilities to cover larger macro blocks such as memory, mixed signal and custom digital cores. Macro blocks require additional pre-analysis steps in order to make fast and accurate characterization feasible. Leveraging a network of distributed CPUs and utilizing Altos' unique "inside view" technology for optimizing characterization runtime, memories and cores can be characterized quickly and easily with the same accuracy and methods as standard cells, including the generation of timing constraints and modeling of current source models for timing and noise.

Large custom macros comprise a large percentage of silicon area on most chips and consequently can often be major contributors to chip performance and power consumption. To validate a design's electrical performance it is essential to have a highly accurate electrical model for each macro equivalent in accuracy of the electrical models used for standard cells and I/Os.

Using pre-packaged models provided by an IP provider or memory compiler may not provide sufficient accuracy especially as the exact context of the macro is not known until it is placed on the chip. The model may be too pessimistic causing overruns in schedule and increased usage of larger or leakier cells in order to close timing. It is also common to operate a macro block at a lower voltage to save power. To get an accurate electrical model that reflects the exact usage of the macro, a design specific and/or instance specific macro block characterization is required.

Bi-modal view characterization

Liberate MX uses both a full block view and partitioned sub-block views to characterize large macro blocks efficiently and accurately. The full block view is used to characterize power and to drive the creation of sub-block partitions. Typically a "fast SPICE" simulator such as CustomSim (Hsim®, NanoSim® and XA), ADiT™, or Ultrasim™ is used for the full block circuit analysis while a traditional SPICE simulator is used for characterizing the sub-blocks. Liberate MX also supports auto-vector creation for digital cores without requiring block level simulation.

Circuit Partitioning

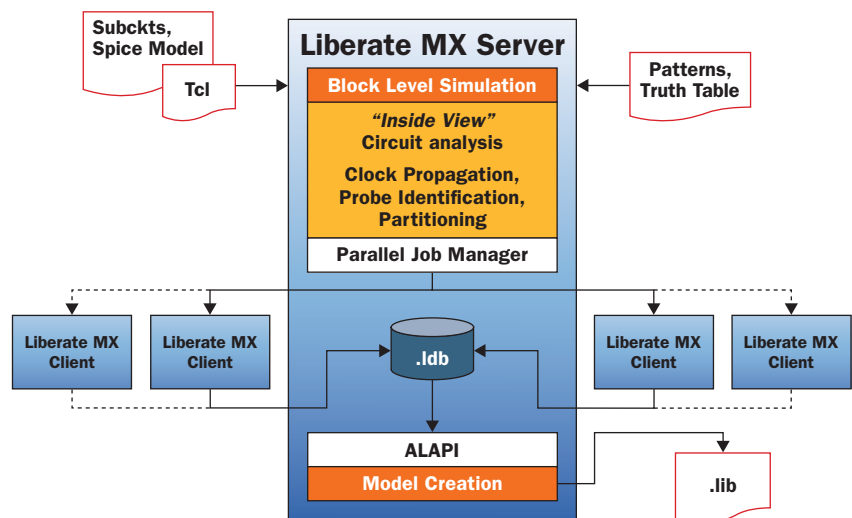
In order to partition each macro, Liberat MX first determines internal measurement points via propagation of clocks signals

and recognition of internal storage elements. Liberat MX uses two distinct techniques for partitioning: static and dynamic.

Static partitions are based solely on circuit topology and are used for fully digital sections of the macro. A typical static partition would be all of the channel connected logic components on the path between a primary input and a first level flip-flop including all the required clock generation circuitry.

Dynamic partitions are derived from a full block transistor level simulation using a pattern sequence or a high level truth table description. From the simulation an active circuit snapshot can be extracted corresponding to the worst-case timing. Dynamic partitioning is useful for characterizing timing arcs that contain analog circuitry such as the clock to output data arcs in embedded memories.

Once a macro has been partitioned into sub-blocks comprising typically a few hundred transistors, Liberat MX submits

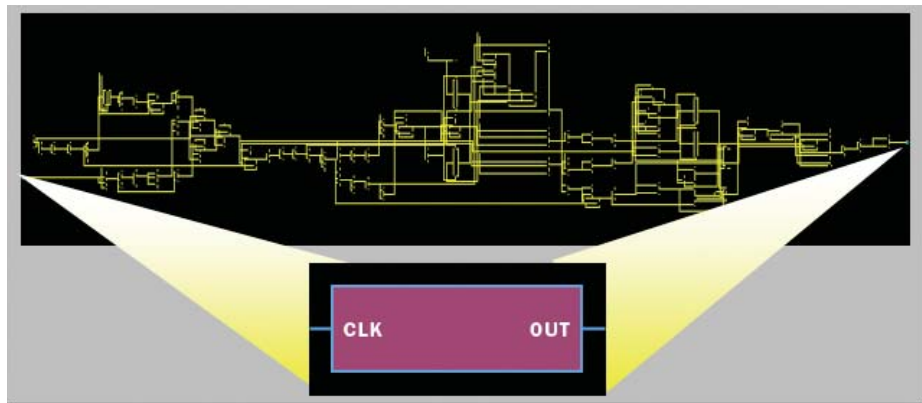


each partition for characterization using either the internal Alspice™ SPICE simulator or an external simulator such as Eldo®, Hspice® or Spectre®.

Library Generation

Leveraging the same characterization techniques with all the same command options as Liberate, each arc of each MX partition is characterized across a distributed network of computers utilizing all the available CPUs. The distribution can be controlled using a job management system or using Liberate’s built in job scheduler. Current source models (CCS/ECSM) for timing, power and noise can also be generated.

After characterization all the characterized library data for each partition is assembled and compressed into a single output library representing the macro in Liberty™ format.



Partition thru a Memory Block from CLK to OUT

Liberate MX is available on:

- RedHat Enterprise Linux 3 update 8 or later, Enterprise Linux 4 update 4 or later
- CentOS 3.8 or later, 4.4 or later

Feature	Benefit
Greatly improves characterization speed and ease of use by automatic partitioning and vector generation	Improves design productivity and reduces power by enabling fast and easy instance specific macro characterization avoiding the margining inherent in compiler or hand generated models
Bi-modal view utilizes both fast SPICE and traditional SPICE	Enables a more cost-effective utilization of simulation tools
Custom measurement support	Easy Memory Compiler integration
Current source models (CCS/ECSM) for timing, power and noise	Improved accuracy with better correlation to Silicon

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